# REMARKS/ARGUMENTS

Applicants acknowledge the rejection of Claims 1, 2, 4 - 10, 12 and 14 - 23 with a right to traverse.  Claims 1, 10 and 12 are amended herein.  Applicants respectfully request further examination and reconsideration of the rejections for the reasons stated below.

## Claim Rejections - 35 U.S.C. §103

Claims 1, 2, 4 - 10, 12 and 14 - 23 were rejected as being allegedly unpatentable over U.S. Patent No. 5,371,878 (hereinafter "Coker") in view of "How Debuggers Work" by Jonathan B. Rosenberg (hereinafter "Rosenberg") and further yet in view of U.S. Patent No. 5,968,135 (hereinafter "Teramoto").  Applicants respectfully traverse in view of the following.

Applicants respectfully submit that the rejection fails to establish a prima facie case of obviousness since the combined references of Coker, Rosenberg and Teramoto fail to teach each and every element of the Claims.

Currently amended independent Claim 1 recites,

> a boot method for synchronizing a microcontroller and a virtual
> microcontroller of an In-Circuit Emulation system in lock-step, comprising:
> in the microcontroller, executing a set of boot code to carry out

initialization; in the virtual microcontroller, executing a set of timing code to enable a lock-step synchronization with the microcontroller, wherein the set of timing code is a dummy code timed to take the same number of clock cycles as the microcontroller uses to execute the set of boot code, wherein the set of timing code is <u>functionally</u> different from the set of boot code, and wherein the set of boot code is stored within the microcontroller and the set of boot code is inaccessible to the virtual microcontroller, and simultaneously halting both the microcontroller and the virtual microcontroller,

as claimed.

According to the rejection, Coker teaches or suggests the claimed features that "the set of timing code is different from the set of boot code" as it allegedly discloses execution of different software on a target-ECS (microcontroller) and a shadow system (virtual microcontroller). However, Applicants respectfully submit that Coker fails to teach or suggest claimed features of currently amended Claim 1 that "the set of timing code is <u>functionally</u> different from the set of boot code."

The rejection states that Coker "explicitly" teaches that the software executed by the target-ECS is different from the software executed by the shadow system as it recites that "[t]hus, rather than receiving input data from an external source and reading the data into complex I/O registers, the shadow system uses the data value and relative time of input events from the target-ECS and writes the value directly to its RAM using its internally generated location," (see column 2, line 63 – column 3, line 1).

However, Applicants respectfully assert that the difference cited by the passage fails to teach or suggest that the software executed by the target-ECS is <u>functionally</u>

different from the software executed by the shadow system. This is readily evident as Coker recites that "[i]n general, this invention uses hardware and software which can "shadow" the execution of a target-ECS in real time operation, within or without a suit of computers, and record only necessary information for later re-creation of the real time scenario, without interfering with the operation of the target-ECS," see column 2, lines 34-39. That is, the software executed by the shadow system in Coker is <u>functionally the same</u> as that of the target-ECS as the shadow system functions to shadow the target-ECS.

Accordingly, Coker "explicitly" discloses the functional equivalence of the software executed by the target-ECS and the software executed by the shadow system in several passages as it recites that "[a] shadow system of this invention executes the same software as the target-ECS from system start-up or reset," see column 2, lines 56-58, that "[t]he shadow system 28 includes and executes the same software and input signals (after being converted by the input filter 22 to unique input events) as the target-ECS12," see column 4, lines 40-44, and that "[t]he shadow system 28 of FIG. 1 has the same CPU and executes the same software as the target-ECS 12," see column 7, lines 66-67. Accordingly, Coker fails to teach or suggest that the software executed by the target-ECS, which corresponds to the microcontroller in Claim 1, is <u>functionally</u> different from the software executed by the shadow system, which corresponds to the virtual microcontroller in Claim 1, as claimed.

Since Coker fails to teach or suggest the claimed features of "the set of timing code is functionally different from the set of boot code," Applicants respectfully submit that Claim 1 overcomes this reference under 35 USC § 103 and is in condition for allowance. The other cited references of Rosenberg and Teramoto fail to solve the deficiencies of Coker as discussed above with respect to Claim 1. Accordingly, Applicants respectfully request the withdrawal of the rejection.

Applicants respectfully submit that dependent Claims 2 and 4 - 9 overcome the rejections of record by virtue of their dependency to Claim 1, and respectfully solicit allowance of these Claims. In addition, Applicants respectfully assert that the combined references fail to teach or suggest the features that "the set of timing code is functionally different from the set of boot code," as recited in Claim 1.

Independent claims 10 and 12 recite at least those features similar to that of Claim 1 and are therefore patentable over the cited references for the same reasons. As such, allowance of independent Claims 10 and 12 is earnestly solicited.

With respect to remaining Claims that depend on Claims 10 and 12, Applicants respectfully assert that the Claims overcome the rejections of record for at least the rationale previously presented with respect to the independent Claims and for the additional features they recite, and respectfully solicit allowance of these Claims.

For the reasons stated above, Applicants earnestly solicit the allowance of

Claims 1, 2, 4 - 10, 12 and 14 - 23.

## CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1, 2, 4 - 10, 12 and 14 - 23 overcome the rejections of record and, therefore, allowance of the Claims is earnestly solicited.

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Respectfully submitted,

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